REMARKS

Claims 1-22 are rejected under 35 U.S.C 102(e) as being anticipated by Jeansonne et al. (Jeansonne, US2004/0205280).

Response:

Applicant asserts that Claims 1-22 are not anticipated by Jeansonne et al. due to the fact that the inventions are structurally different. Jeansonne et al. teaches a bridge system that can connect multiple devices at the peripheral end (output end) while using a single communication interface at the host end. This is in contrast to the present invention, where a bridge system connecting a single device at the peripheral end to multiple interfaces at the host end, is presented. A quick comparison of Fig.2 of Jeansonne et al. to Fig 4. of the present invention will clearly and concisely illustrate this structural difference. For this reason, and reasons listed in the following, the applicant kindly requests that the Examiner reconsider the rejections placed on the proposed claims.

With specific regard to the rejection of Claim 1, applicant asserts that the prior art does not require the reception of a predetermined protocol initialization signal for the activation of the corresponding bridge chip. For example, Jeansonne et al. show in Fig. 9 that control signal 80 is driven by a Voltage source 122 and a pull-down resistor 124, connected to the arbitrary control input of the component connector 132, 134. This simple hardware circuit ensures that the bridge will be shared with the relevant component 62, 64 as long as a physical connection to the bridge is present, and is therefore not reliant on a predetermined protocol initialization signal. Similar operation is further explained in paragraph [0022], in which Jeansonne et al. teach that the automatic endpoint selector 65 responds to a "component event". This is further described as "the selector 65 can respond to the insertion of a selected one of the components 32 and 34 and enable the bridge chip 58 or 60

corresponding to that selected and inserted component." Additionally, the component event is described in paragraph [0015] as "a selected component may become active (and others inactive) by removing one component and mutually exclusively inserting the selected component into a component bay. The automatic endpoint selector may comprise a variety of simple switches and a control signal corresponding to a component event. For example, the automatic endpoint selector may comprise a multiplexor, an isolation switch, or a variety of hardware switches". From the above discussion, applicant asserts that Jeansonne et al. do not teach "enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal", as stated in Claim 1 of the present invention.

Also regarding Claim 1, applicant asserts that the prior art does not teach each activation circuit disabling the corresponding bridge chip after a power on or after a hardware reset. Jeansonne et al. show in Fig. 4 that the enable circuits of Mulit-Component Device 40 are driven in parallel from a control signal 80, with one enabling device having a series inverter 78 at the input. Therefore, since the inputs of the enable circuits are logically opposed, this ensures that one of the End-Points 54, 56 must remain active upon a power on or hardware reset. Furthermore, for the reasons stated above with respect to the component event and the circuit illustrated in Fig 9 of the prior art, the bridge of the prior art will remain active regardless of a power on or hardware reset as long as this physical connection is established. The operational examples and teachings of Jeansonne et al. are in contrast to the present invention as claimed in claim 1. Specifically, that the activation circuit is for "disabling the corresponding bridge chip after a power-on, a hardware reset, or physical disconnection from the host and enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal" (emphasis added). Additionally, the above comments are also applicable to the rejections of independent Claims 8, 13, and 18. Reconsideration of claims 1, 8, 13, and 18 is respectfully requested. As the remaining claims 2-7, 9-12, 14-17, and 19-22 are dependent claims, if the independent claims are found allowable, so too should the dependent claims. Further comments regarding the patentability the dependent claims is

given below.

In regards to Claim 4, applicant asserts that the prior art does not teach setting the pins of the device bus interface to float when the bridge chip is disabled under reset or power-up conditions. Consider the embodiment as shown by Jeansonne et al. in Fig 9. If a component 62,64 is attached to the receptacle 108, it will gain access to the bridge interface for reasons stated in [0030]-[0031]. However, if a reset occurs during a physical connection to the receptacle 108, it will clearly re-gain control of the bridge interface afterwards for reasons listed in [0030]-[0031], although the bridge chip was temporarily disabled through a reset. This is in contrast to the present invention as claimed in Claim 4. Claim 4 states that "when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface". Therefore, upon a reset or power-up, control to the device bus interface will be lost. Similar comments are also applicable to the corresponding rejections of Claims 10, 14, and 20. Reconsideration of claims 4, 10, 14, and 20 is respectfully requested.

In regards to Claim 6, applicant asserts the prior art does not teach that the enabled bridge chip retains control of the device bus interface until a power-off, a hardware reset, or the bridge chip has been physically disconnected from the host. In particular, the prior art only suggests enabling and disabling according to a control signal that is determined according to a component event. As shown in Fig 9 of Jeanesson at al., control signal 80 is received from the component outputs 132, 134. Therefore, if the component is removed in the prior art, a toggle in the control signal may occur, causing the bridge chip to lose control of the device bus interface. This is in contrast to the present invention as claimed in Claim 6. Specifically, that the "the enabled bridge chip retains control of the device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host." According to the limitations claimed in Claim 6, the enabled bridge chip retains control of the device bus interface regardless of the attachment or detachment of

different devices 25 in Fig.4 of the present invention. Similar comments are also applicable to the corresponding rejections of Claims 16 and 22. Reconsideration of claims 6, 16, 22 is respectfully requested.

In regards to Claim 12, applicant asserts the prior art does not teach the device comprising "an original bus interface capable of communications between the device and the host computer system utilizing an original bus interface when all of the bridge chips are disabled." As shown in Fig.4 and described in paragraph [0024] of the present invention, "when a device bus interface 40A exists, the device can still be used via the device bus interface 40A if desired because neither of the bridge chips 105 or 110 are necessary to support this arrangement." This is in contrast to the figures and descriptions of Jeanssone et al. where if all the bridge chips are disabled, the host has no way to communicate with the device. Reconsideration of Claim 12 is respectfully requested.

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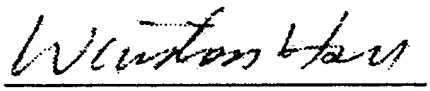

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